REMARKS and ARGUMENTS

Claims 1-53 were presented for examination. Claims 22, 23, 47, and 50 has been cancelled. Claim 35 has been amended to correct the spelling of predicated as suggested by the examiner.

Objections to the Specification

Applicant has amended paragraph [0011] to start with Fig. 3 instead of Fig.. 3 as suggested by the examiner.

Claim Rejections USC § 112

Examiner rejects claims 1-29 under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement, stating destination registers being distinct could not be found in the specification. However, applicant's claim 1 includes, "at least one of the plurality of micro-operations indicate a single destination register that is distinct from the destination registers indicated by the other micro-operations." As can be seen from paragraph 0037, the register "temp" is a distinct destination register to be hold qp appended to r1, which is distinct from the other destination register r1, as described in paragraphs 0038 to 0040.

Similarly, in table 1, for each predicated instruction, at least one distinct destination register for a micro-operation is illustrated. For example, in 2. temp1 and temp2 are destination registers for the append micro-operations that are distinct from the other micro-operation destination registers, i.e. r1 and r3. In reference to claim 24, a similar limitation of at least one of the plurality of standard micro-operations indicates a single destination register that is distinct.

Other reference to differing micro-operation destination registers may be seen throughout the specification.

In addition, applicant's claim 19 includes a first ..., a second..., and a third micro-operation ..., which is also illustrated by example in Table 1, as well as throughout the specification. Therefore, applicant respectfully submits that claim 1-29 have adequate support in the specification as illustrated above.

Claim Rejections -35 USC § 102(b)

The Office Action has rejected Claims 1-6, 19-22, 24-26, 28, 30-40 and 53 under 35 U.S.C. § 102(b) as being anticipated by U.S. Pat. No. 6,170,052 to Morrison (referred to hereinafter as "Morrison"). "[F]or anticipation under 35 U.S.C. 102, the reference must teach *every aspect* of the claimed invention ..." MPEP 706.02 (emphasis added). "The identical invention must be shown *in as complete detail as contained in the ... claim.*" *Richardson v., Suzuki Motor Co.*, 868 F. 2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989) (emphasis added).

Morrison discloses at column 5 lines 46-53 the following:

> FIG. 6 is a flowchart illustrating the steps of a method **66** for executing conditional instructions with special predicated sequences on the out-of-order processor **50** of FIG. 5. At block **68**, the method begins by decoding a conditional instruction into a predicate evaluating micro-op **31** and an associated pair of conditional micro-ops **32**, **33** having the form illustrated in FIG. 3. At block **70**, the predicate and pair of conditional micro-ops are sequentially sent from one of the decoders **54**, **56** to the renamer **58**. At block **72**, the logical destination register of the first conditional micro-op **32** of the predicate **30** is renamed with a physical register. At block **74**, a micro-op received at the renamer **58** is identified as the second conditional micro-op **33** associated with the same predicated sequence **30**. At block **76**, the physical register that renames the logical destination register of the first conditional micro-op **32** is assigned to be the physical register that renames the logical destination register of the second conditional micro-op **33** of the pair **32**, **33**. At block

As can be seen, Morrison discloses decoding a predicated instruction into a predicate and **paired conditional micro**-ops, and in block 76 teaches renaming the destination register of the second micro-op of the pair to **the same physical register**. In other words, both micro-ops 32, 33 have the same destination register, i.e. the same physical register. As a result, micro-ops 32,33, one of which or both fulfills the predicated instruction's basic function, have the same destination register.

Claim 1. In contrast, applicant's claim 1 recites, in part, "at least one of the plurality of micro-operations indicate **a single destination register that is distinct from the destination registers** indicated by the other micro-operations," (Claim 1 as amended, in part).

In one embodiment described in applicant's specification at paragraphs 0034 – 0040, a single predicated instruction, such as (qp) add r1 = r2,r3 is decomposed into three micro-operations: (1) append temp = r1, qp; (2) add r1 = r2,r3; and (3) cmov r1=temp, r1. Here, the destination register temp for the append micro-operation is distinct from the destination register of the add micro-operation, r1. In contrast, with applicant's disclosure, Morrison discloses pairing a first micro-operation, such as retaining the old value of r1 that is stored in the temp destination register in applicant's disclosure, with a second micro-operation of add r1 = r2,r3. Here, both the destination registers for the two conditional paired operations in Morrison are the same physical register, i.e. r1.

Applicant's claim 1 includes at least one of the plurality of micro-operations indicate a single destination register that is distinct, unlike Morrison where the conditional pair of micro-operations are specifically renamed to the same physical register. Applicant's dependency chain is potentially longer than Morrison's disclosure, however, applicant's distinct destination registers allows for more parallel processing in an Out-Of-Order (OOO) processor. Therefore, applicant respectfully submits that claim 1 and its dependent claims 2-18 are now in condition for allowance.

Claim 19. Morrison fails to disclose, teach or suggest all the claim limitations of Claim 19. For example, amended Claim 19 recites, in part, "a first micro-operation to associate a predicate value with a first value from a first register in a second register, the second register being different from the first register, a second micro-operation to store a second value in the first register, and a select micro-operation to select the first or second value to be stored in the first register based on the predicate value associated with the first value in the second register." Morrison merely discloses pairing conditional micro-ops and associating each of the pair with the same physical register, not micro-operations with different destination registers, i.e. the first micro-operation with the second register and the second micro-operation with the first register, as disclosed in applicant's claim 19. Therefore, applicant respectfully submits that claim 19-21 are in condition for allowance for at least the reasons stated above.

Claim 24. Morrison fails to disclose, teach or suggest all the claim limitations of Claim 24. For example, amended Claim 24 recites, in part, "at least one of the plurality of standard micro-operations indicates a single destination register that is distinct from the destination registers indicated in ~~of~~ the other standard micro-operations of the plurality of standard micro-operations." (amended Claim 24, in part). At paragraph 00039 an embodiment of a standard micro-operation is illustrated, i.e. a "standard micro-op addresses the basic operation indicated by the instruction 120. As stated above, Morrison does not teach or suggest at least one of the plurality of standard micro-operations indicating a single destination register that is distinct. In fact, Morrison explicitly discloses that the paired conditional micro-ops are renamed to the same physical register.

Claim 30. Morrison fails to disclose, teach or suggest all the claim limitations of Claim 30. For example, amended Claim 30 recites, in part, "a third micro-operation to select the first value or the second value to be stored in the second destination register based on a predication value." (Claim 30, in part, emphasis added). Morrison only discloses executing a predicate micr-op, but does not disclose a third micro-op to select the first value (from the first destination register) or the second value (from the second destination register) to be stored in the second destination register based on a predication value, as disclosed in applicant's claim 30. Therefore, applicant respectfully requests that claim 30 and its dependent claims 31-46, 48-49, and 51-53 are in condition for allowance for at least the reasons stated above.

If there are any additional charges, please charge Deposit Account No. 50-0221. If a telephone interview would in any way expedite the prosecution of the present application, the Examiner is invited to contact David P. McAbee at (503) 712-4988.

Respectfully submitted,
Intel Corporation

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/David P. McAbee/Reg. No. 58,104/
David P. McAbee
Reg. No. 58,104

Intel Corporation
M/S JF3-147
2111 NE 25th Avenue
Hillsboro, OR 97124
Tele – 503-712-4988
Fax – 503-264-1729